CY2300A Low Power Sub-1GHz RF Transceiver

Revision: V0.4

1. Overview

The CY2300A is an ultra-low power, highly integrated, high-performance RF transceiver suitable for Sub-1GHz band wireless applications. It features a wide input voltage range of 1.8V to 3.6V, a maximum transmit power of up to 20dBm, and a minimum sensitivity of -120dBm. It supports various modulation schemes such as OOK and (G)FSK, as well as multiple data packet formats and encoding/decoding methods, offering the flexibility to meet the needs of various low-power, ad-hoc network applications.

2. Key Features

- Operating Mode: Standalone RF transceiver chip, communicates with the host controller via an SPI interface.
- Frequency Range: 240 - 960 MHz
- Transmit Power: Maximum 20 dBm
- Receive Sensitivity:

  -120 dBm @ 1.2kbps / 433.92MHz

  -100 dBm @ 100kbps / 433.92MHz

- Saturated Receive Power: 20 dBm
- Data Rate Range: 0.5 – 300 kbps (Configurable)
- Modulation Schemes: OOK, (G)FSK, (G)MSK
- Operating Voltage: 1.8V – 3.6V
- Operating Current:
- Transmit Current:

  75mA @ +20dBm, 433.92 MHz, FSK

  24mA @ +13dBm, 433.92 MHz, FSK

- Receive Current:

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8.3mA @ 433.92 MHz, FSK (High Sensitivity)

7.8mA @ 433.92 MHz, FSK (Low Power)

- Sleep Current:

  300 nA, Deep Sleep

  800 nA, Normal Sleep

- Special Features:
  - Supports Direct Mode and Packet Mode, configurable packet handling mechanism and 64-Byte FIFO.
  - Supports Forward Error Correction (FEC), Data Whitening encoding/decoding.
  - Supports Automatic Frequency Calibration (AFC).
  - Supports Clear Channel Assessment (CCA).
  - Supports MESH ad-hoc network applications.
  - Supports Frequency Hopping applications.
- Complies with FCC/ETSI standards, RoHS standard.
- Package: QFN16

3. Application Areas

- Smart City Applications
- Smart Photovoltaic Scenarios
- Smart Metering and Measurement Systems
- Home and Building Automation
- Remote Control, Alarm, and Security Systems
- Wireless Lighting Control Systems
- Industrial Remote Control Systems
- Wireless Data Transmission
- Multi-function Remote Controls

4. Package Type

CY2300A uses a QFN16 package.

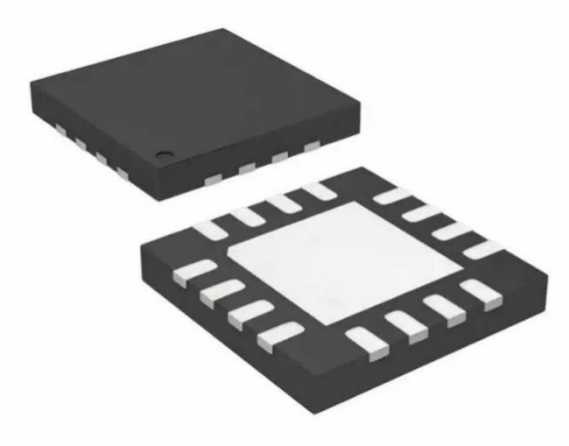

Figure 1 CY2300A Package Diagram

5. Pin Configuration and Definition

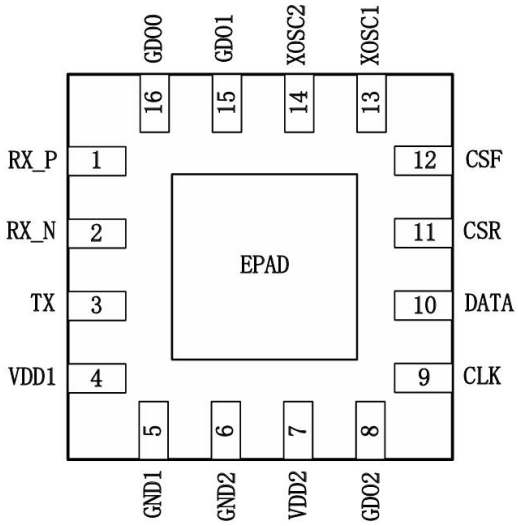

Figure 2 CY2300A Pinout Diagram

Pin	Pin Name	I/O	Description
1	RX_P	I	Receiver signal input
2	RX_N	I	Receiver signal input
3	TX	O	Transmitter signal input

4	VDD1	I	Connect to positive power supply
5	GND1	I	Ground
6	GND2	I	Ground
7	VDD2	I	Connect to positive power supply
8	GDO2	IO	Configurable I/O ports
9	CLK	IO	SPI clock
10	DATA	IO	SPI data
11	CSR	I	SPI Register Chip Select
12	CSF	I	SPI-FIFO Chip Select
13	XOSC1	I	Crystal input
14	XOSC2	I	Crystal input
15	GDO1	IO	Configurable I/O ports
16	GDO0	IO	Configurable I/O ports
EPAD	GND	I	Ground

Table 1: CY2300A Pin Description

6. System Block Diagram & Functional Description

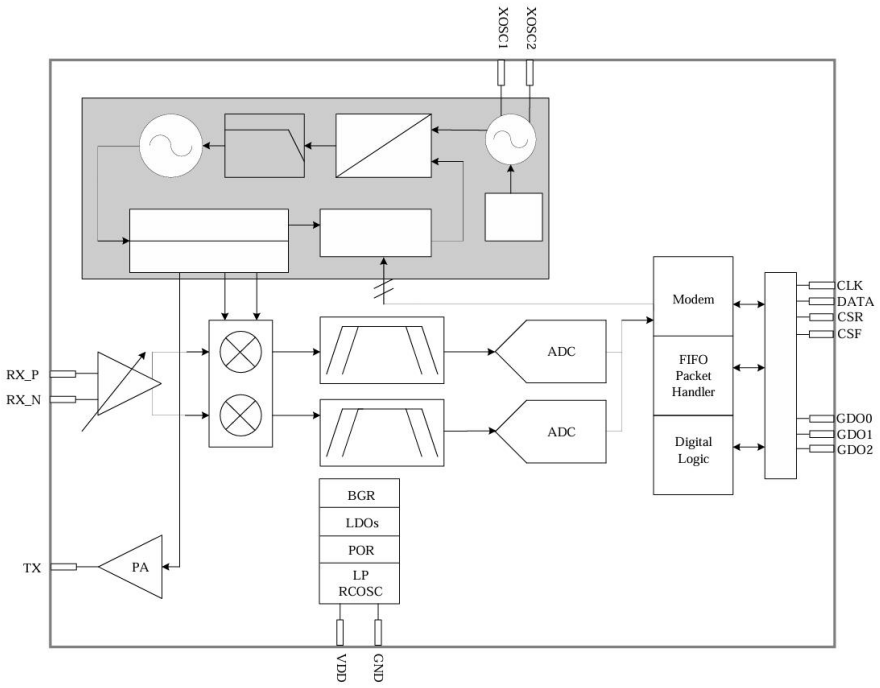

Figure 3 CY2300A System Block Diagram

The CY2300A is a fully integrated transceiver designed with mixed-signal technology, primarily consisting of key units such as the Transmitter, Receiver, Digital Baseband, Power Management Module, and Frequency Synthesis Module.

6.1 Transmitter

The transmitter is mainly composed of a Power Amplifier (PA) and a Frequency Synthesizer (PLL). The PLL employs a Fractional-N structure with a Sigma-Delta Modulator (SDM). The PA uses a Class-E digital amplifier structure. The maximum transmit power can reach 20dBm, configurable via registers.

6.2 Receiver

The receiver is mainly composed of a Low-Noise Amplifier (LNA), Mixer (MIXER), Band-Pass Filter (BBPF), and Analog-to-Digital Converter (ADC). An Automatic Gain Control (AGC) circuit provides an excellent dynamic range.

6.3 Digital Baseband

The digital baseband consists of Modulation/Demodulation, Packet Processing, Logic Control, and SPI Control Interface modules, managing the chip's operational states.

6.4 Power Management Module

This module includes a Bandgap Reference (BGR), LDO, Power-On Reset (POR), and Low-Power RC Oscillator (LP RCOSC) for power regulation and management.

6.5 Frequency Synthesis Module

The frequency synthesizer uses a Fractional-N PLL with an LC VCO. A 26MHz crystal provides the reference clock. Crystal selection must consider parasitic capacitance to avoid performance degradation.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Voltage	V_{DD}	-0.3		3.9	V
Input Voltage	V_{IN}	-0.3		3.9	V
Storage Temperature	T_{STG}	-50		150	℃
Welding Temperature	T_{SDR}			255	℃
Chip Junction Temperature	T_J	-40		125	℃
ESD Level	(HBM)	-4		+4	KV
Latch-up Current		-100		+100	mA

Table 2: Absolute Maximum Ratings

7.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Working Voltage	V_{DD}	1.8	3.3	3.6	V
Working Temperature	T_{OP}	-40		85	℃

Table 3: Recommended Operating Conditions

Note: RF chips are sensitive devices; ESD protection must be considered during use.

7.3 RF Parameters

Test Conditions: VDD=3.3V, 25°C, Tx Power=20dBm

7.3.1 Transmitter Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Frequency Range	FRF	240		960	MHz

Output Power	POUT	-10	13	20	dBm
Power Step	PSTEP		1		dBm
Transmission Rate	OOK	0.5		40	kbps
	(G)FSK	0.5		300	kbps
Transmission Frequency Deviation	FDEV	2		200	KHz
Phase Noise 433.92MHz	10KHz		-96		dBc/Hz
	100KHz		-98		dBc/Hz
	500KHz		-119		dBc/Hz
	1MHz		-129		dBc/Hz
	10MHz		-140		dBc/Hz
Phase Noise 868.35MHz	10KHz		-92		dBc/Hz
	100KHz		-92		dBc/Hz
	500KHz		-113		dBc/Hz
	1MHz		-121		dBc/Hz
	10MHz		-135		dBc/Hz
Harmonic suppression	H2433.92		-40		dBm
	H3433.92		-50		dBm
	H2868.35		-45		dBm
	H3868.35		-50		dBm
Bandwidth Usage	OBW(99%)		60		KHz

Table 4: Transmitter Parameters

7.3.2 Receiver Parameters

Parameter	Symbol	Min	Typ	Max	Unit

Receive rate	OOK	0.5		40	kbps
	(G)FSK	0.5		300	kbps
Receive Frequency Deviation	FDEV	2		200	kHz
Receiver Sensitivity 433.92MHz	1.2kbps/5kHz		-120		dBm
	1.2kbps/10kHz		-119		dBm
	2.4kbps/10kHz		-118		dBm
	2.4kbps/20kHz		-119		dBm
	4.8kbps/10kHz		-115		dBm
	4.8kbps/20kHz		-116		dBm
	9.6kbps/9.6kHz		-113		dBm
	9.6kbps/19.2kHz		-114		dBm
	20kbps/10kHz		-111		dBm
	20kbps/20kHz		-112		dBm
	50kbps/25kHz		-106		dBm
	50kbps/50kHz		-105		dBm
	100kbps/50kHz		-100		dBm
	100kbps/100kHz		-100		dBm
	200kbps/50kHz		-90		dBm
	200kbps/100kHz		-96		dBm
	300kbps/100kHz		-91		dBm
	300kbps/150kHz		-93		dBm
Receiver Sensitivity 868.35MHz	1.2kbps/5kHz		-117		dBm
	1.2kbps/10kHz		-118		dBm
	2.4kbps/10kHz		-116		dBm

	2.4kbps/20kHz		-117		dBm
	4.8kbps/10kHz		-113		dBm
	4.8kbps/20kHz		-114		dBm
	9.6kbps/9.6kHz		-112		dBm
	9.6kbps/19.2kHz		-113		dBm
	20kbps/10kHz		-109		dBm
	20kbps/20kHz		-110		dBm
	50kbps/25kHz		-104		dBm
	50kbps/50kHz		-103		dBm
	100kbps/50kHz		-97		dBm
	100kbps/100kHz		-99		dBm
	200kbps/50kHz		-91		dBm
	200kbps/100kHz		-95		dBm
	300kbps/100kHz		-89		dBm
	300kbps/150kHz		-92		dBm
Receive Saturation Power				20	dBm
Receive Bandwidth		50		500	kHz

Table 5: Receiver Parameters

7.4 Power Consumption

Test Conditions: VDD=3.3V, 25°C

Parameter	Symbol	Min	Typ	Max	Unit
Received Current (High Performance)	315M,10kbps/10kHz		7.92		mA
	433M,10kbps/10kHz		8.22		mA
	868M,10kbps/10kHz		8.36		mA

	915M,10kbps/10kHz		8.45		mA
Received Current (Low Power Consumption)	315M,10kbps/10kHz		7.49		mA
	433M,10kbps/10kHz		7.77		mA
	868M,10kbps/10kHz		8.0		mA
	915M,10kbps/10kHz		8.0		mA
Emission Current	433M, 20dBm		76		mA
	433M,13dBm		25		mA
	433M,10dBm		18		mA
	868M,20dBm		88		mA
	915M,20dBm		90		mA
Sleep Current	Normal sleep		0.8		uA
	Deep sleep		0.3		uA

Table 6: Power Consumption

7.5 Crystal Oscillator Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Crystal frequency	FXOSC		26		MHz
Accuracy			20		ppm
Load Capacitor	CLOAD		15		pF
Equivalent Resistance	Rm		40		Ω

Table 7: Crystal Specification

7.6 Typical Performance

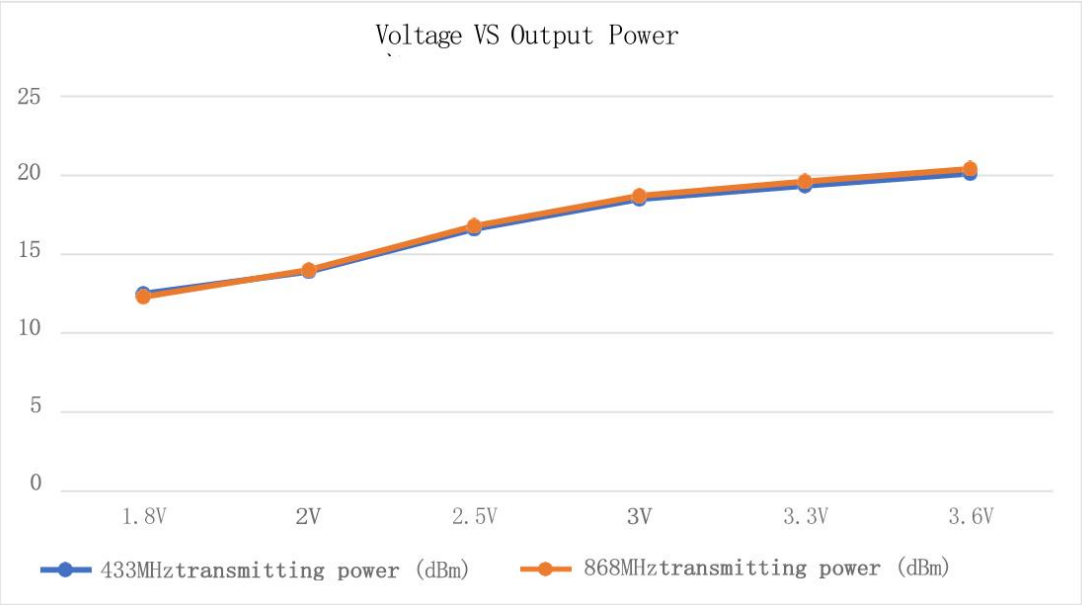

Figure 4: Transmit Power vs. Supply Voltage

Test conditions: 25℃, VDD = 3.3V reference, 20dBm configuration

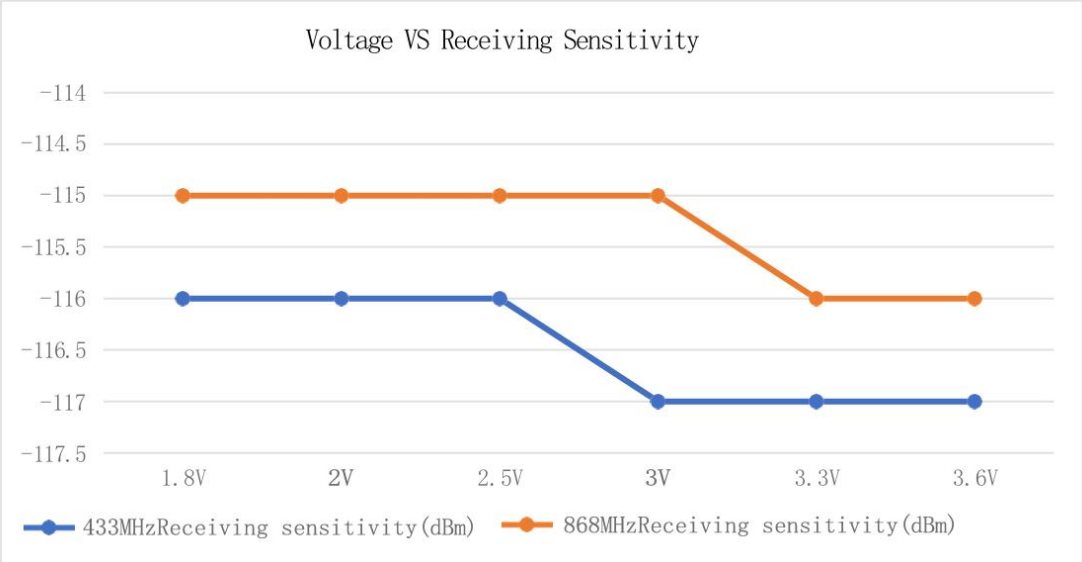

Figure 5: Receive Sensitivity vs. Supply Voltage

Test conditions: 25℃, VDD = 3.3V reference, 2.4kbps, 10kHz frequency offset

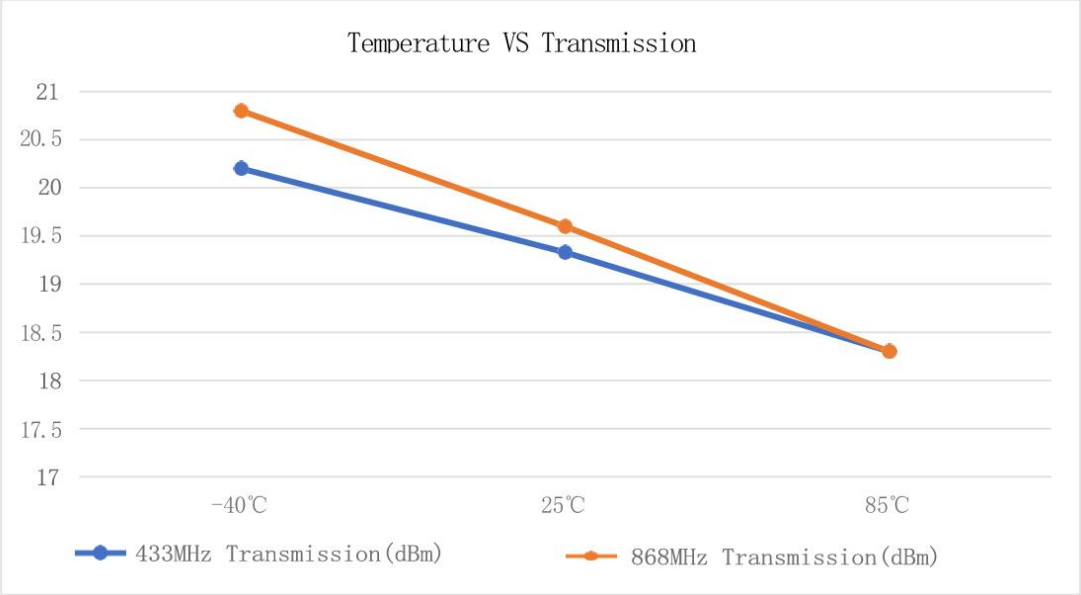

Figure 6: Transmit Power vs. Temperature

Test conditions: VDD = 3.3V, 20 dBm configuration

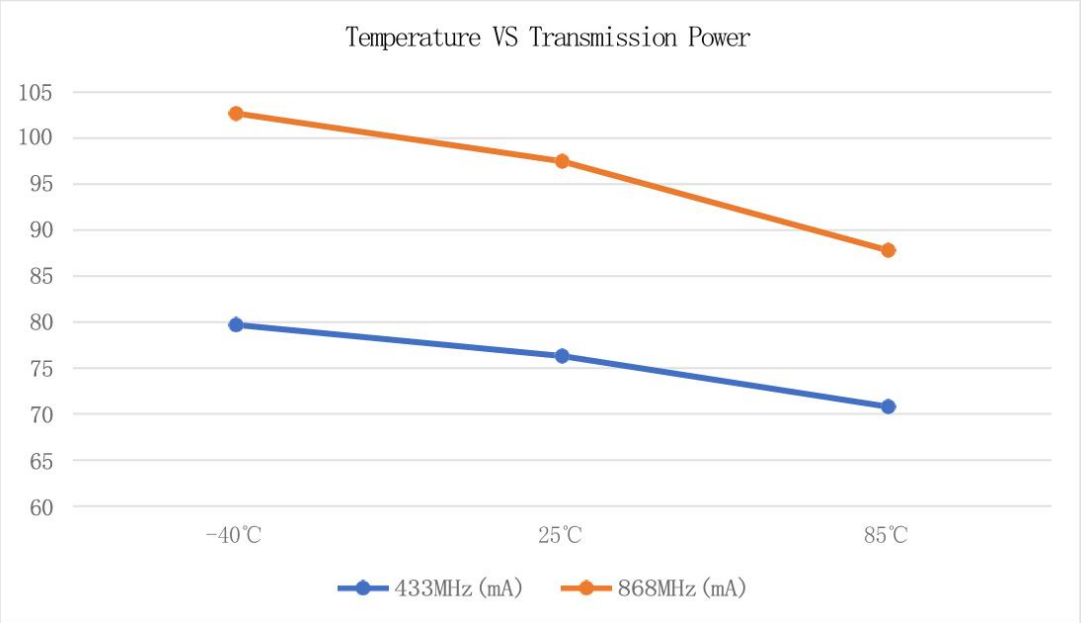

Figure 7: Transmit Current vs. Temperature

Test conditions: VDD = 3.3V, 20 dBm configuration

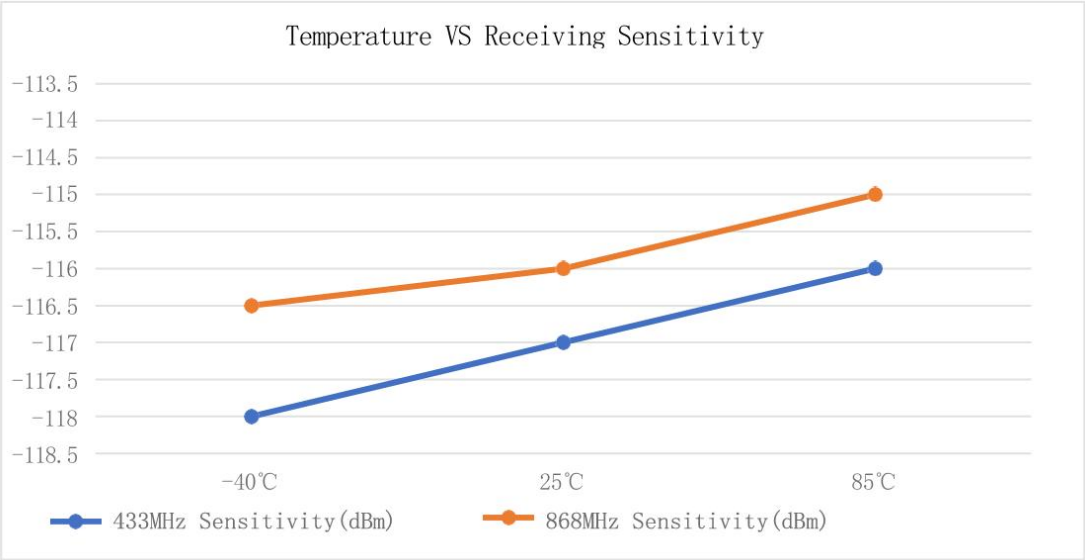

Figure 8: Receive Sensitivity vs. Temperature

Test conditions: VDD = 3.3V, 2.4kbps, 10kHz frequency offset

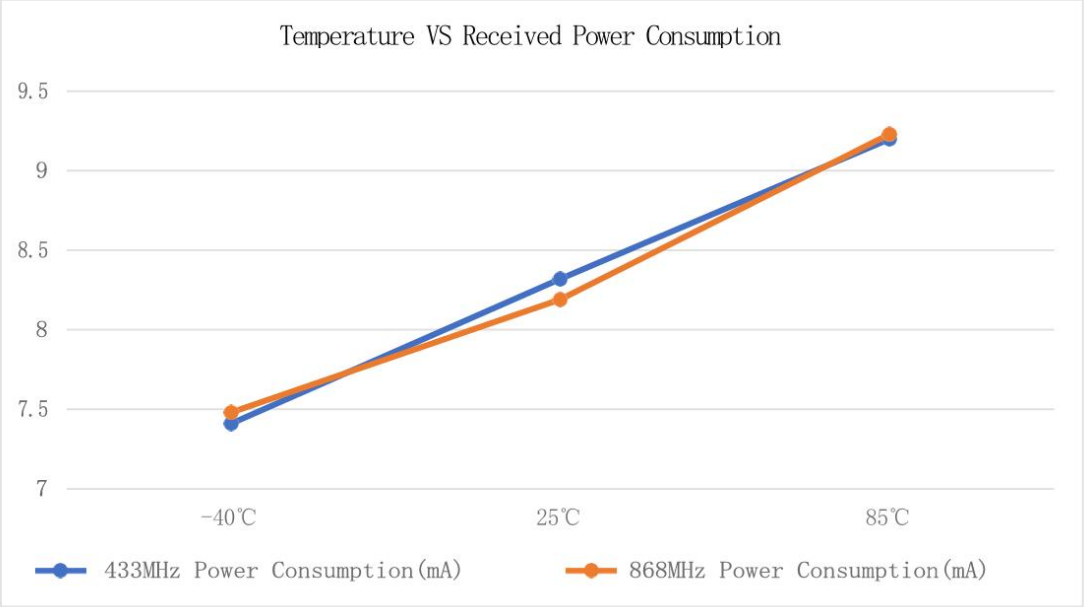

Figure 9: Receive Current vs. Temperature

Test conditions: VDD = 3.3V, 2.4kbps, 10kHz frequency offset

8. Typical Applications

8.1 Typical Applications of CY2300A- Direct-13dBm

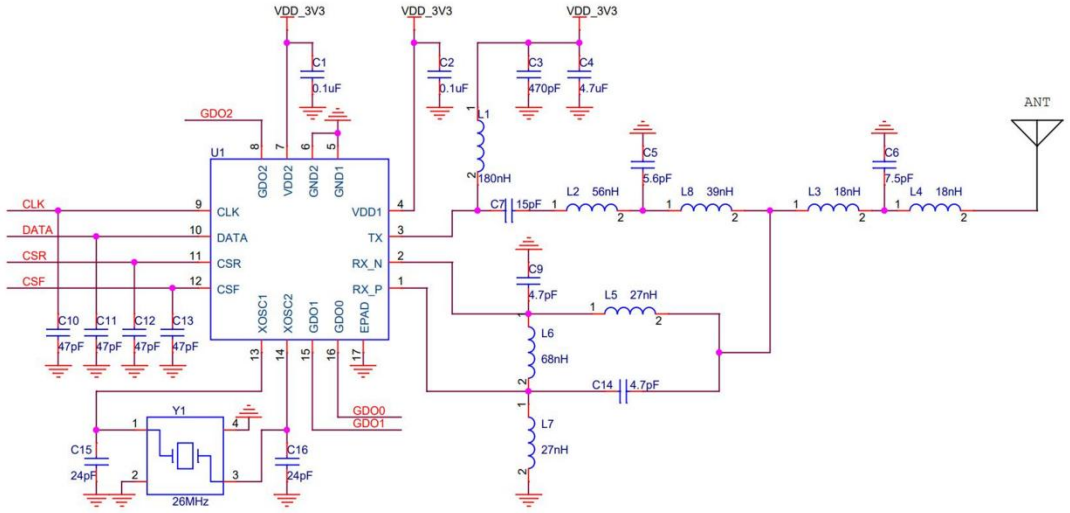

Figure 10: CY2300A-433MHz-Direct-13dBm Typical Application Circuit

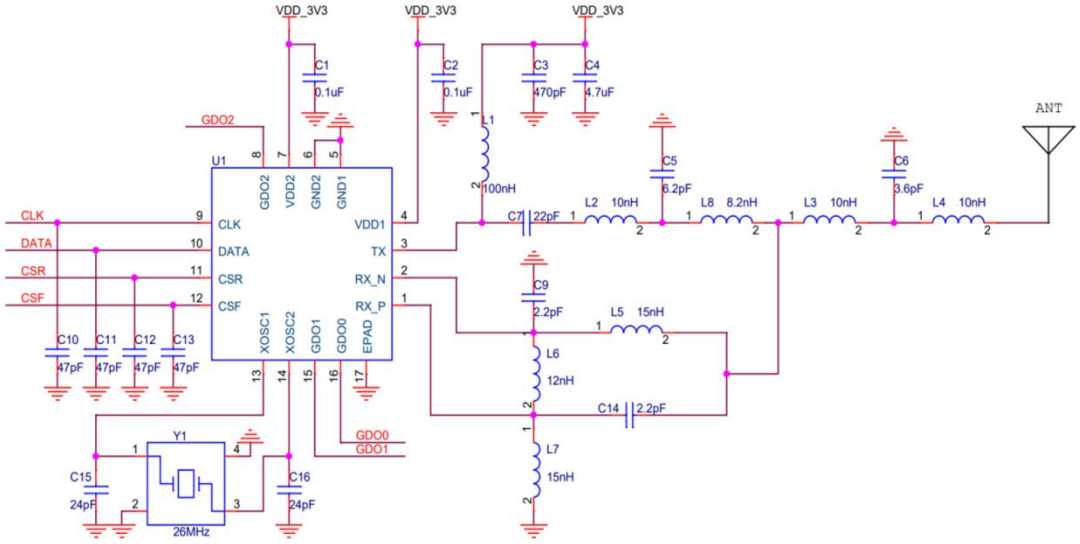

Figure 11: CY2300A-868MHz-Direct-13dBm Typical Application Circuit

8.2 Typical Applications of CY2300A-Direct-20dBm

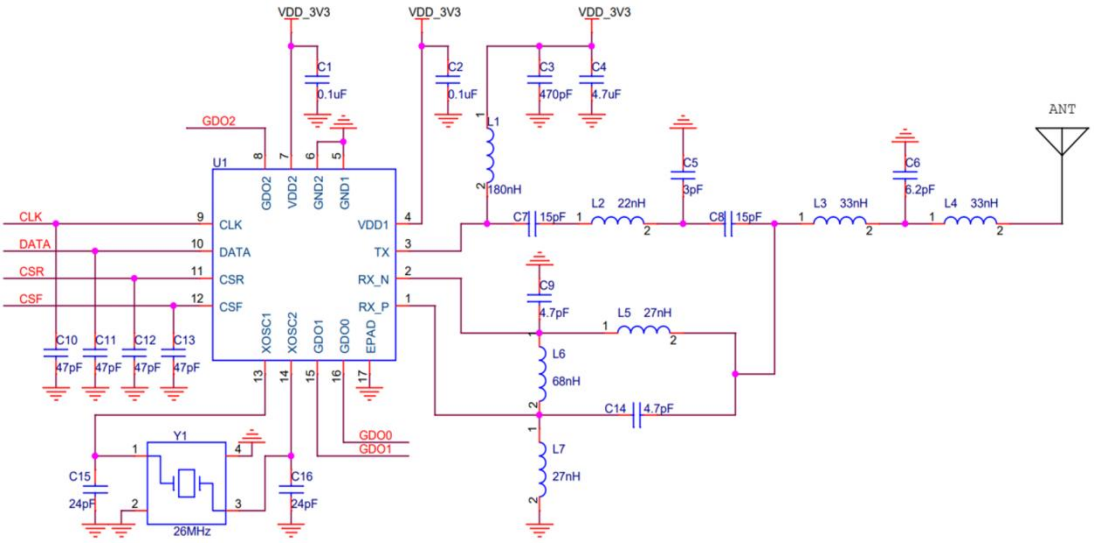

Figure 12: CY2300A-433MHz-Direct-20dBm Typical Application Circuit

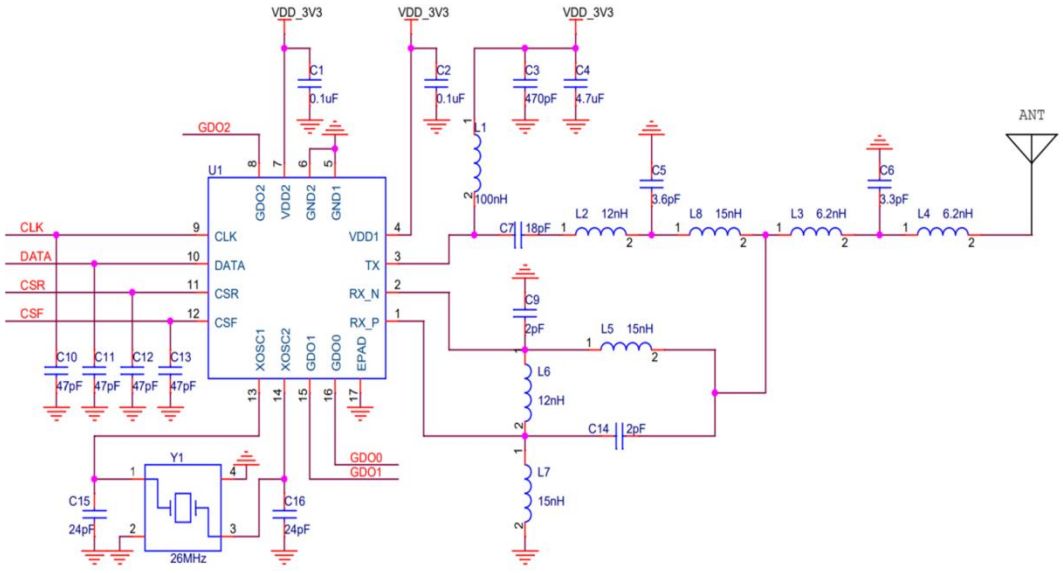

Figure 13: CY2300A-868MHz-Direct-20dBm Typical Application Circuit

8.3 Typical Applications of CY2300A- SPDT- 20dBm

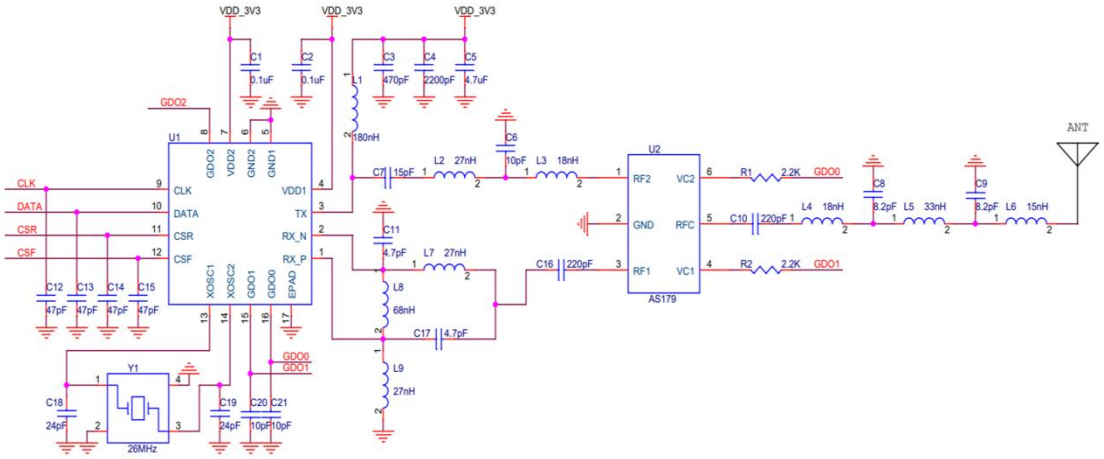

Figure 14: CY2300A-433MHz-SPDT-20dBm Typical Application Circuit

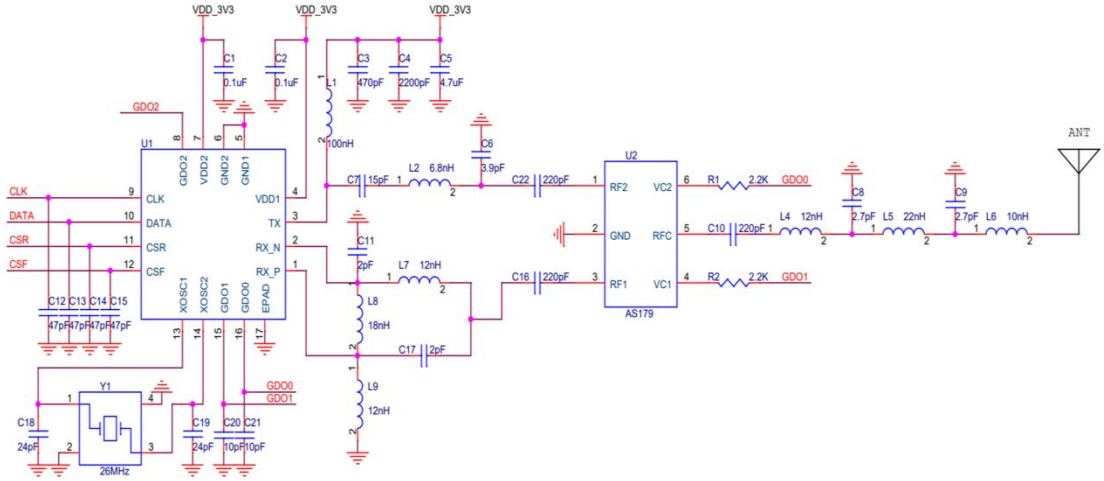

Figure 15: CY2300A-868MHz-SPDT-20dBm Typical Application Circuit

9. Package Dimensions

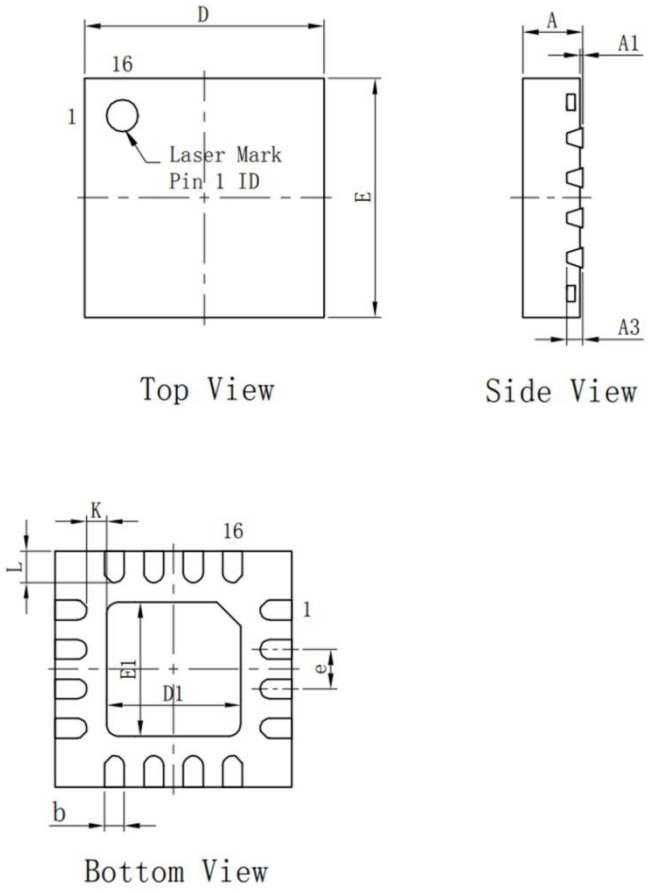

Figure 16 QFN16 Package Dimension Diagram

Symbol	Dimension (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.023		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10

D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.50 BSC		
K	0.20	--	--
L	0.30	0.40	0.50

Table 8: QFN16 Package Dimensions (mm)